Appl. No.: 10/602,982 Amdt. dated 02/06/2006

Reply to Office action of September 6, 2005

REMARKS

Status of Claims

In the Office Action, Claims 1-10, 12-15 and 17-19 were noted as pending in the application and all claims were rejected under 35 U.S.C. 103(a). The rejections are addressed separately below.

Rejection of Claims 1- 9, 12, 13 and 17 under 35 U.S.C. § 103(a) based on Chavarkar (U.S. Publication No. 2002/0167023 A1) in view of Wolter (U.S. Patent No. 4,677,457) in further view of Murota et al. (U.S. 2002/0109135 A1)

On page 2, item 3 of the Office action, Claims 1-9, 12, 13 and 17 were rejected under 35 U.S.C. § 103(a) based on <u>Chavarkar</u> (U.S. 2002/0167023 A1) in view of <u>Wolter</u> (U.S. Patent No. 4,677,457) in further view of Murota et al. (U.S. 2002/0109135 A1).

For the following and other reasons already made of record, it is submitted that Claims 1-9, 12, 13 and 17 are patentable over the cited prior art.

A. The Chavarkar Publication

The Chavarkar publication discloses in paragraphs [0012]-[0013] that the use of an aluminum nitride (AlN) and gallium nitride (GaN) system for forming a high electron mobility transistor (HEMT) is disadvantageous because of the lattice mismatch if the layer is made too thick (i.e., greater than 50 Å), then the lattice mismatch causes problems with ohmic contacts, reduces material quality, decreases device reliability, and makes the AlN layer more difficult to grow. To overcome these problems, Chavarkar discloses a Group III nitride based HEMT device based on aluminum gallium nitride (AlGaN) and gallium nitride (GaN) (e.g., paragraph [0014]). The HEMT device is formed on a substrate consisting of sapphire, silicon carbide, gallium nitride, or silicon (paragraph [0015]). Chavarkar states that the spontaneous and piezoelectric polarization of wurtzite group III-nitrides are found to be approximately 10 times larger than in conventional Group III-V and II-VI semiconductor compounds, implying that Group III-V and II-VI semiconductor compounds are unsuitable for use in its HEMT device [0026].

B. Claims 1-9, 12, 13, and 17 Patentably Distinguish Over the Prior Art

Claim 1 of the subject application recites that the claimed HEMT device comprises "a channel layer being composed of a II-VI compound semiconductor zinc oxide (ZnO)." As noted

Amdt. dated 02/06/2006

Reply to Office action of September 6, 2005

in the Office action, <u>Chavarkar</u> fails to disclose a channel layer composed of II-VI compound semiconductor zinc oxide (ZnO). In fact, <u>Chavarkar</u> implies that Group II-VI semiconductor devices are unsuitable for its invention, thus not only failing to disclose the claimed invention, but suggesting that it is undesirable despite applicant's work which demonstrates that HEMT devices embodying the claimed invention can be used to make high-quality HEMT devices. Thus, <u>Chavarkar</u> not only fails to disclose the claimed invention, it teaches away from it.

Wolter fails to disclose the deficiencies of <u>Chrvarkar</u>. Wolter is relied upon as disclosing use of ZnO as a possibility for a material to be used to create a two-dimensional electron gas in a HEMT device. However, in column 7, line 57-column 8, line 8, Wolter expressly states:

Suitable materials are, for instance, other III-V components and mixed crystals thereof, for example InP, InAs, InSb, GaP, GaSb, etc., II-VI compounds and mixed crystals thereof, for example CdSe, CdTe, CdS, ZnSe, ZnO, etc., <u>or</u> elementary semiconductors such as Ge and Si. *Emphasis added*.

Thus, properly interpreted, Wolter teaches that Group III-V compounds or mixed crystals, or Group II-VI compounds or mixed crystals thereof, or elementary semiconductors, can be used to form its semiconductor device. Wolter does not state that materials from Group II-VI like ZnO or MgZnO should be used with Group III-V materials like Group III-nitrides. Neither Wolter nor any other reference relied upon by the Examiner discloses MgZnO. Thus, Chavarkar and Wolter, whether considered alone or in combination, fail to disclose a channel layer composed of a II-VI compound semiconductor zinc oxide combined with a gate insulating layer composed of Group III-nitride compound semiconductor or a magnesium zinc oxide (MgZnO) quantum well structure, or both. Thus, because both Chavarkar and Wolter "teach away" from the claimed invention, their combination is respectfully traversed because a person of ordinary skill would not have been motivated to combine them as done in the Office action. In re Leshin, 277 F.2d 197 (C.C.P.A. 1960) is inapposite because inter alia the express statements noted above in the cited art "teach away" from the modifications and combinations made in the Office action. Claim 1 as amended would not have been obvious to a person of ordinary skill in the art considering these patents whether alone or in combination because such patents "teach away"

Amdt. dated 02/06/2006

Reply to Office action of September 6, 2005

from the claimed invention and thus fail to disclose it. Therefore, it is submitted that Claim 1 as amended is patentable over the prior art.

Furthermore, neither Chavarkar nor Wolter disclose "a gate contact disposed in proximity to, but not in contact with, said channel layer" and "a gate insulating layer disposed between and in contact with said gate contact and said channel layer and composed of at least one of a Group-III nitride compound semiconductor and a magnesium zinc oxide (MgZnO) quantum well structure, said gate insulating layer having side walls, said gate contact positioned between the sidewalls of said gate insulating layer so that sides of said gate contact face the side walls of said gate insulating layer" as recited in Claim 17 as amended. Neither Chavarkar nor Wolter disclose this limitation, whether considered alone or in combination, nor is there any disclosure in the prior art suggesting modification in any way that would meet all of the limitations of Claim 17. Murota also fails to disclose this feature of the claimed invention because it does not disclose a gate insulating layer with the claimed compositions in combination with the channel layer and gate contact of the claimed composition, nor is there any suggestion that would have led the person of ordinary skill in the art to combine its teachings with Chavarkar or Wolter. Accordingly, impermissible hindsight has been used in which the Applicant's disclosure, not the prior art, has been used as the basis to provide the motivation to modify or combine the citations. See In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988). When properly considered, Claim 1 is patentable over the prior art of record.

Claims 2-9, 12 and 13 depend from Claim 1 as amended and include all of the limitations of that Claim. Thus, for at least the reasons stated above with respect to Claim 1, Claims 2-9, 12 and 13 are patentable over the prior art.

Claim 17 recites steps of "defining a channel layer composed of a II-VI compound semiconductor zinc oxide (ZnO)" and "forming a gate insulating layer in contact with said channel layer and composed of at least one of a Group-III nitride compound semiconductor and a magnesium zinc oxide (MgZnO) quantum well structure, said gate insulating layer formed with side walls." The prior art fails to disclose steps of defining a ZnO channel layer and forming a gate insulating layer in contact with a channel layer that is composed of either or both of a Group-III nitride compound semiconductor and a MgZnO quantum well structure, as claimed in

Amdt. dated 02/06/2006

Reply to Office action of September 6, 2005

Claim 17. None of the art relied upon in the Office action discloses forming a gate insulating layer of MgZnO or a Group-III nitride, on a defined ZnO channel layer, as recited in the claimed invention. Moreover, the prior art fails to disclose "forming a gate contact disposed on and in contact with said gate insulating layer and positioned between said side walls, said gate contact formed to have sides facing said side walls of said gate insulating layer, said gate contact formed in proximity to, but not in contact with, said channel layer" as recited in Claim 17. There is no disclosure in the prior art that would have led one to combine Chavarkar, Wolter and Murota as done in the Office action. To the contrary, the cited art teach away from the claimed invention and each other.

Rejection of Claim 10 under 35 U.S.C. § 103(a) based on Chavarkar, Wolter, Murota and Shanfield (U.S. Patent No. 5,880,483)

On page 5, item 5 of the Office action, Claim 10 was rejected under 35 U.S.C. 103(a) based on Chavarkar, Wolter, Murota and Shanfield. Shanfield is relied upon as disclosing a passivation layer 36 on a gate electrode 24, source electrode 20, and drain electrode 22.

It is submitted that there is no teaching or suggestion in Chavarkar, Wolter, Murota and Shanfield that would have led the person of ordinary skill in the art to combine these citations as done in the Office action. Accordingly, impermissible hindsight has been used in which the Applicant's disclosure, not the prior art, has been used as the basis to provide the motivation to modify or combine the citations. See In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

In addition, Claim 10 depends from Claim 1 as amended and therefore includes all of the limitations of that Claim. Because Shanfield fails to disclose the deficiencies of Chavarkar, Wolter, and Murota as noted above with respect to Claim 1, Applicant submits that Claim 10 is patentable over the prior art of record due at least to its dependency from Claim 1. Thus, for at least the reasons stated above with respect to Claim 1 as amended, Applicant submits that Claim 10 is patentable over the prior art or record.

Amdt. dated 02/06/2006

Reply to Office action of September 6, 2005

Rejection of Claim 14, 15 and 19 under 35 U.S.C. § 103(a) based on Chavarkar, Wolter, Murota and Nishikawa et al. (U.S. Patent No. 6,323,053)

On page 6, item 6 of the Office action, Claims 14, 15, and 19 were rejected under 35 U.S.C. 103(a) based on Chavarkar, Wolter, Murota and Nishikawa. Nishikawa is relied upon to disclose a ZnO substrate with a c-surface.

It is submitted that there is no teaching or suggestion in the prior art that would have led the person of ordinary skill in the art to combine Suzuki, Wolter or Nishikawa as done in the Office action. Accordingly, impermissible hindsight has been used in which the Applicant's disclosure, not the prior art, has been used as the basis to provide the motivation to modify or combine the citations. See In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

The Office action cites In re Leshin, 277 F.2d 197 (C.C.P.A. 1960) for the proposition that to select a known material on the basis of its suitability for the intended use of the claimed device is a matter of obvious design choice. However, with reference to FIG. 4, Nishikawa discloses a structure with a c-surface ZnO substrate 11, a terminating hydrogen layer 12, a gallium selenide (GaSe) layer 13, a nitrogen-substituted buffer layer 23, and a gallium nitride (GaN) layer 14. The purpose of this complex structure of intervening layers 12, 13, 14 between the GaN layer 14 and the ZnO substrate 11 is to relax the stress between them due to lattice mismatch. It does not disclose the desirability of providing a ZnO channel layer on a ZnO substrate, on which is formed either a Group III nitride compound semiconductor or a magnesium zinc oxide (MgZnO) quantum well structure, as claimed in Claims 14, 15 and 19. In the case of the channel layer being a Group III nitride compound semiconductor, the pseudomorphic strain between the ZnO channel layer supported by the ZnO structure is what produces the two-dimensional electron gas of the semiconductor device. Nishikawa "teaches away" from this configuration, instead instructing that one must use layers 12, 13, 14 to relax strain between the nitride and layers. This would reduce effectiveness or lead to inoperability of the claimed device. As to the case in which the channel layer is composed of a MgZnO quantum well structure, neither Nishikawa nor any other citation discloses MgZnO, let alone a quantum well structure made with it. Thus, In re Leshin is inapposite here: the material of the cited art, namely c-surface ZnO, is not used being use for the intended purpose of the claimed invention.

Amdt. dated 02/06/2006

Reply to Office action of September 6, 2005

Moreover, Chavarkar expressly excludes a ZnO substrate as an option, stating instead that its HEMT device can be formed on a substrate made from a material from the group consisting of sapphire, silicon carbide, gallium nitride and silicon. Thus, the combination relied upon in making this rejection fails for this additional reason.

In addition, Claims 14 and 15 depend from Claim 1 as amended and therefore includes all of the limitations of that Claim. Because Nishikawa fails to disclose the deficiencies of Chavarkar, Wolter, Murota and Nishikawa as noted above with respect to Claim 1, Applicant submits that Claims 114 and 15 are patentable over the prior art of record due to its dependency from Claim 1.

Claim 19 depends from Claim 17 and includes all limitations of that Claim. Because the Nishikawa fails to disclose the deficiencies of Chavarkar, Wolter and Murota as noted above with respect to Claim 17, Applicant submits that Claim 19 is patentable over the prior art of record due to its dependency from Claim 17.

Rejection of Claim 18 under 35 U.S.C. § 103(a) based on Chavarkar, Wolter, Murota, and Ando (U.S. Patent No. 6,429,467 B1)

On page 7, item 6 of the Office action, Claim 18 was rejected under 35 U.S.C. 103(a) based on Chavarkar, Wolter and Murota, in further view of Ando. Ando is relied upon to disclose a gate insulating layer formed by metal organic chemical vapor deposition (MOCVD). However, Claim 18 recites that "...the gate insulating layer is formed by metal organic chemical vapor deposition (MOCVD)." 35 U.S.C. 103(a) requires that the claim be considered as a whole, not in piecemeal fashion. Due to the other claim limitations, Claim 18 effectively recites using MOCVD to form a gate insulating layer composed of Group III nitride compound semiconductor or a magnesium zinc oxide (MgZnO) quantum well structure, in contact with a ZnO channel layer. Ando does not disclose use of MOCVD in the claimed manner. Therefore, Applicant submits Claim 18 is patentable over the prior art of record.

Furthermore, Claim 18 depends from Claim 17 and thus includes all of the limitations of that Claim. Because Ando fails to disclose the deficiencies of Chavarkar, Wolter and Murota as noted above with respect to Claim 17, it is submitted that Claim 18 is patentable over the prior art of record.

Appl. No.: 10/602,982 Amdt. dated 02/06/2006

Reply to Office action of September 6, 2005

Conclusion

It is submitted that Claims 1-10, 12-15 and 17-19 are patentable over the prior art of record. Accordingly, reconsideration of the Claims in light of the above remarks, withdrawal of the rejections, and a Notice of Allowance for all pending Claims, are earnestly solicited.

It is not believed that extensions of time or fees for net addition of claims are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 CFR § 1.136(a), and any fee required therefore (including fees for net addition of claims) is hereby authorized to be charged to Deposit Account No. 16-0605.

Respectfully submitted,

Jon M. Jurgovan

Registration No. 34,633

Customer No. 00826 ALSTON & BIRD LLP

Bank of America Plaza 101 South Tryon Street, Suite 4000 Charlotte, NC 28280-4000 Tel Atlanta Office (404) 881-7000 Fax Atlanta Office (404) 881-7777

"Express Mail" mailing label number EV 355488833 US Date of Deposit February 6, 2006

I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to:

Mail Standard Property Commissioner for Potents, P.O. Poy 1450, Alexandric, VA 23213, 1450.

Mail Stop Americanent, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

Shelley Victoria